WHAT IS CLAIMED IS:

1. A method comprising:

in response to a first signal indicating the execution of a breakpoint by a processor, suspending execution of a peripheral and saving the state of the peripheral;

continuing execution of the breakpoint by the processor in response to receiving a second signal indicating that the state of the peripheral has been saved; and

restoring the saved state of the peripheral in response to a third signal indicating that execution of the breakpoint by the processor has been completed.

2. The method of claim 1 comprising resuming normal execution of the processor in response to a signal indicating that the saved state has been restored.

3. The method of claim 1 comprising resuming normal execution of the peripheral in response to a signal indicating that the processor has resumed normal execution.

4. The method of claim 1 comprising setting a register to control whether generation of the second signal is to be based on the state of the peripheral.

5. The method of claim 1 comprising setting a register to control whether generation of a signal indicating that the

saved state has been restored is to be based on the state of the peripheral.

6. The method of claim 1 comprising triggering the breakpoint in response to a condition associated with occurrence of an instruction being executed by the processor.

7. A system comprising:

a processor;

a first computer-readable medium storing instructions that, when applied to the processor, cause the processor to:

generate a first signal indicating execution of a breakpoint,

continue execution of the breakpoint in response to receiving a second signal, and

generate a third signal indicating that execution of the breakpoint has been completed;

a peripheral coupled to the processor;

a second computer-readable medium storing instructions that, when applied to the peripheral, cause the peripheral to:

suspend execution and save a state of the peripheral, in response to receiving the first signal,

restore the state of the peripheral, in response to receiving the third signal; and

a digital logic circuit to generate the second signal indicating that the state of the peripheral has been saved, the digital logic circuit coupled to the processor and the peripheral.

8. The system of claim 7 wherein the first computer-readable medium includes instructions that cause the processor to:

resume normal execution in response to receiving a fourth signal, and

generate a fifth signal indicating that the processor has resumed normal execution; and

wherein the second computer-readable medium includes instructions that cause the peripheral to resume normal execution, in response to receiving the fifth signal; and

wherein the digital logic circuit is configured to generate the fourth signal indicating that the saved state of the peripheral has been restored.

9. The system of claim 8, further comprising:

a second processor;

a third computer-readable medium storing instructions that, when applied to the second processor, cause the second processor to:

suspend execution and save a state of the second processor, in response to receiving the first signal,

restore the state of the second processor, in response to receiving the third signal, and

resume normal execution, in response to receiving the fifth signal; and

the digital logic circuit configured to:

generate the second signal indicating that the state of the second processor has been saved, and

generate the fourth signal indicating that the saved state of the second processor has been restored.

10. The system of claim 7 including a system on a chip (SOC).

11. The system of claim 7 including a debugging tool coupled to the system to debug the system.

12. The system of claim 7 wherein the digital logic circuit comprises a register to control whether generation of the second signal is to be based on the state of the peripheral.

13. The system of claim 7 wherein the state identifies a state of internal registers associated with the peripheral.

14. The system of claim 7 wherein the processor operates at a clock rate different than the peripheral.

15. An apparatus comprising:

a processor having a computer-readable medium storing instructions that, when applied to the processor, cause the processor to:

generate a signal indicating execution of a breakpoint,

continue execution of the breakpoint in response to receiving a signal indicating that the state of a peripheral has been saved, and

generate a signal indicating that execution of the breakpoint has been completed.

16. The apparatus of claim 15 wherein the computer-readable medium includes instructions that cause the processor to resume normal execution in response to a signal indicating that the saved state has been restored.

17. An article comprising a computer-readable medium that stores computer-executable instructions for causing a computer system to:

generate a signal indicating execution of a breakpoint;

continue execution of the breakpoint in response to receiving a signal indicating that the state of a peripheral has been saved; and

generate a signal indicating that execution of the breakpoint has been completed.

18. The article of claim 17 wherein the computer-readable medium stores computer-executable instructions for causing a computer system to resume normal execution of the processor in response to a signal indicating that the saved state has been restored.

19. An apparatus comprising:

a peripheral having a computer-readable medium storing instructions that, when applied to the peripheral, cause the peripheral to:

suspend execution and save a state of the peripheral, in response to receiving a signal indicating execution of a breakpoint, and

restore the state of the peripheral, in response to receiving a signal indicating that execution of the breakpoint has been completed.

20. The apparatus of claim 19 wherein the computer-readable medium includes instructions that cause the peripheral to resume normal execution of the peripheral in response to a signal indicating that a processor has resumed normal execution.

21. An article comprising a computer-readable medium that stores computer-executable instructions for causing a computer system to:

suspend execution and save a state of the peripheral, in response to receiving a signal indicating execution of a breakpoint, and

restore the state of the peripheral, in response to receiving a signal indicating that execution of the breakpoint has been completed.

22. The article of claim 21 wherein the computer-readable medium stores computer-executable instructions for causing a computer system to resume normal execution of the peripheral in response to a signal indicating that a processor has resumed normal execution.

23. An apparatus comprising:

one or more signal lines used to receive signals and to send signals; and

a processor configured to:

generate a signal indicating execution of a breakpoint,

continue execution of the breakpoint in response to receiving a signal on a signal line indicating that the state of a peripheral has been saved, and

generate a signal on a signal line indicating that execution of the breakpoint has been completed.

24. The apparatus of claim 23 wherein the processor is configured to resume normal execution in response to a signal indicating that the saved state has been restored.

25. An apparatus comprising:

one or more signal lines used to receive signals and to send signals; and

a peripheral configured to:

suspend execution and save a state of the peripheral, in response to receiving a signal indicating execution of a breakpoint, and

restore the state of the peripheral, in response to receiving a signal indicating that execution of the breakpoint has been completed.

26. The apparatus of claim 25 wherein the peripheral is configured to resume normal execution in response to a signal indicating that a processor has resumed normal execution.